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First Named Inventor	Frankie F. Roohparvar
Serial No.	09/627,682
Filing Date	July 28, 2000
Group Art Unit	2186
Examiner Name	Behzad Peikari
Confirmation Number	3555
Attorney Docket No.	400.008US01

TRANSMITTAL FORM UNDER 37 CFR 1.10

(LARGE ENTITY)

Title: SYNCHRONOUS NON-VOLATILE MEMORY SYSTEM

Mail Stop: APPEAL BRIEF - PATENTS
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Enclosures

The following documents are enclosed:

X Appeal Brief (in triplicate) (27 pgs.);
X A check in the amount of $330.00 (Appeal Brief);
X a return postcard.

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APPEAL BRIEF

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Table of Contents

I. Introduction

Appellant filed a Notice of Appeal to the Board of Patent Appeals and Interferences on June 18, 2004. Three copies of this Appeal Brief are hereby timely filed on August 10, 2004, and are accompanied by a fee in the amount of $330.00 as required under 37 C.F.R. § 1.17(c).

II. Real Party in Interest

The present application has been assigned to Micron Technology, Inc., a corporation organized and existing under and by virtue of the laws of the State of Delaware, and having an office and principal place of business at 8000 S. Federal Way, Boise, ID 83706, in an assignment recorded on July 28, 2000, (Reel 010976, Frame 0546).

III. Related Appeals and Interferences

There are no other appeals or interferences known to Appellant which will have a bearing on the Board's decision in the present appeal.

IV. Status of the Claims

Claims 1, 2 and 34 are pending in the application and are the subject of this appeal. Claims 3-26 were subject to a restriction requirement and have been cancelled without prejudice. Claims 27-33 and 35-38, added in the Response filed on March 3, 2003, depend from rejected claims 1, 2 and 34 and were withdrawn by the Examiner as being directed to an unelected invention. The Appellant has noted that one or more of the rejected claims 1, 2 and 34 may be generic to claims 27-33 and 35-38 and has reserved the right to request consideration of withdrawn claims 27-33 and 35-38 if a generic claim is allowed as provided by 37 CFR 1.141, listing claims 27-33 and 35-38 as withdrawn.

In the Final Office Action mailed January 24, 2003 and Advisory Action mailed May 19, 2004 claims 1, 2 and 34 were rejected under 35 U.S.C. §102(b) as being anticipated by Bacon et al. (U.S. Patent 5,440,632). See Appendix for claim set.

V. Status of Amendments

An amendment after final has been filed in this case and denied entry by the Examiner.

VI. Summary of the Invention

A synchronous DRAM (SDRAM) is a type of DRAM that can run at much higher clock speeds than conventional DRAM memory. SDRAM synchronizes itself with a CPU's bus and is capable of running at 100 MHZ, about three times faster than conventional FPM (Fast Page Mode) RAM, and about twice as fast EDO (Extended Data Output) DRAM and BEDO (Burst Extended Data Output) DRAM. SDRAM's can be accessed quickly, but are volatile. Many computer systems with synchronous memory systems, such as SDRAM, are designed to operate using SDRAM, but would benefit from non-volatile memory with a compatible synchronous interface.

The present invention provides methods and apparatus for implementing a synchronous non-volatile memory (such as a synchronous Flash memory), that can operate in a manner similar to and compatible with conventional volatile synchronous memories and memory systems, such as SDRAM. In particular, the claims at issue in the present Application include a computer system that comprises a memory controller and a synchronous non-volatile memory device coupled to the memory controller via a main memory bus. The synchronous non-volatile memory device has external interconnects arranged in a manner that correspond to interconnects of a synchronous dynamic random access memory device. In one embodiment, the synchronous non-volatile memory device has a command interface comprising a write enable connection (WE#) to receive a write enable signal, a column address strobe connection (CAS#) to receive a column address strobe signal, a row address strobe connection (RAS#) to receive a row address strobe signal, and a chip select connection (CS#) to receive a chip select signal.

See, e.g., Application Page 2, Line 11 to Page 3, Line 20; Page 6, Line 10 to Page 7, line 8; Page 45, Line 18 to Page 47, Line 14; and Figs. 1A and 32.

VII. Issue

The question presented in this appeal is whether the Examiner erred in rejecting claims 1, 2 and 34 under 35 U.S.C. §102(b) as being anticipated by Bacon et al. (U.S.

Patent 5,440,632); and objecting to the submitted formal drawings as not complying with 37 C.F.R. §1.84(u)(1) for improper labeling of the views.

VIII. Grouping of Claims

Claims 1, 2 and 34 are grouped by independent claims 1 and 34 and stand or fall on their own merit for the reasons detailed below. In addition, dependent claim 2, describing synchronous non-volatile memory interface and depending from independent claim 1 also stand on its own merit for the reasons detailed below. Each of these claims is patentably distinct, as explained herein.

IX. Arguments

A. Rejection of Claims 1, 2 and 34 under 35 U.S.C. §102(b)

i. The Applicable Law

35 U.S.C. §102

35 U.S.C §102 states, in part:

> A person shall be entitled to a patent unless —
> . . .
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States.
> . . .

The Manual of Patent Examining Procedure (MPEP) reflects this statute and the supporting case law in MPEP §2131 which states:

> **MPEP §2131 Anticipation — Application of 35 U.S.C. 102(a), (b), and (e)**
>
> **TO ANTICIPATE A CLAIM, THE REFERENCE MUST TEACH EVERY ELEMENT OF THE CLAIM**
>
> "***A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.***" *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the . . . claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an *ipsissimis verbis* test, i.e., identity of terminology is not required. In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). *{Emphasis Added}*

As stated in MPEP §2111 and supported by case law, in interpreting the claims at issue in examination, the Examiner must give the broadest reasonable interpretation consistent with the specification. In this the Examiner applies to verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account definitions afforded by the written description contained in applicant's specification. MPEP §2111, states in part:

> **MPEP §2111 Claim Interpretation; Broadest Reasonable Interpretation**
> **CLAIMS MUST BE GIVEN THEIR BROADEST REASONABLE INTERPRETATION**
>
> ***During patent examination, the pending claims must be "given the broadest reasonable interpretation consistent with the specification."*** Applicant always has the opportunity to amend the claims during prosecution, and broad interpretation by the examiner reduces the possibility that the claim, once issued, will be interpreted more broadly than is justified. *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969). . . . See also *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997) (The court held that the PTO is not required, in the course of prosecution, to interpret claims in applications in the same manner as a court would interpret claims in an infringement suit. Rather, the ***"PTO applies to verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in applicant's specification."***).
>
> ***The broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach.*** *In re Cortright*, 165 F.3d 1353, 1359, 49 USPQ2d 1464, 1468 (Fed. Cir. 1999) . . . *{Emphasis Added}*

As stated in MPEP §2111.01 and supported by case law, the claims are broadly interpreted during examination utilizing the "plain meaning" of the words, defined as the meaning given to the terms by those of ordinary skill in the art, unless applicant has provided a clear definition in the specification. MPEP §2111.01 states, in part:

> **MPEP §2111.01 Plain Meaning**
> **THE WORDS OF A CLAIM MUST BE GIVEN THEIR "PLAIN MEANING" UNLESS THEY ARE DEFINED IN THE SPECIFICATION**

> While the meaning of claims of issued patents are interpreted in light of the specification, prosecution history, prior art and other claims, this is not the mode of claim interpretation to be applied during examination. ***During examination, the claims must be interpreted as broadly as their terms reasonably allow. This means that the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification.*** *In re Zletz*, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989) *{Emphasis Added}*
>
> . . .
>
> **"PLAIN MEANING" REFERS TO THE MEANING GIVEN TO THE TERM BY THOSE OF ORDINARY SKILL IN THE ART**
>
> ***When not defined by applicant in the specification, the words of a claim must be given their plain meaning. In other words, they must be read as they would be interpreted by those of ordinary skill in the art.*** *In re Sneed*, 710 F.2d 1544, 218 USPQ 385 (Fed. Cir. 1983) *{Emphasis Added}*
>
> . . .
>
> **APPLICANT MAY BE OWN LEXICOGRAPHER**
>
> ***Applicant may be his or her own lexicographer as long as the meaning assigned to the term is not repugnant to the term's well known usage.*** *In re Hill*, 161 F.2d 367, 73 USPQ 482 (CCPA 1947). Any special meaning assigned to a term "must be sufficiently clear in the specification that any departure from common usage would be so understood by a person of experience in the field of the invention." *Multiform Desiccants Inc. v. Medzam Ltd.*, 133 F.3d 1473, 1477, 45 USPQ2d 1429, 1432 (Fed. Cir. 1998). *{Emphasis Added}*

Inherent elements of a prior art reference may also be used in rejecting claims under 35 U.S.C. §102 or §103. To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art. Once the examiner makes a prima facie case for an element being inherent, the burden shifts to the applicant to refute the case for inherency by reasoning or by providing extrinsic evidence. This is stated in MPEP §2112 and supported by case law. MPEP §2112 states in part:

> **MPEP §2112 Requirements of Rejection Based on Inherency; Burden of Proof**
>
> ***The express, implicit, and inherent disclosures of a prior art reference may be relied upon in the rejection of claims under 35 U.S.C. 102 or 103.*** "The

inherent teaching of a prior art reference, a question of fact, arises both in the context of anticipation and obviousness." *In re Napier* 55 F.3d 610, 613, 34 USPQ2d 1782, 1784 (Fed. Cir. 1995)(affirmed a 35 U.S.C. 103 rejection based in part on inherent disclosure in one of the references). See also *In re Grasselli*, 713 F.2d 731, 739, 218 USPQ 769, 775 (Fed. Cir. 1983). *{Emphasis Added}*

. . .

EXAMINER MUST PROVIDE RATIONALE OR EVIDENCE TENDING TO SHOW INHERENCY

The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993)(reversed rejection because inherency was based on what would result due to optimization of conditions, not what was necessarily present in the prior art); *In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). "***To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'*** " *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)(citations omitted).

. . .

"***In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art.***" *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original) (Applicant's invention was directed to a biaxially oriented, flexible dilation catheter balloon (a tube which expands upon inflation) used, for example, in clearing the blood vessels of heart patients). The examiner applied a U.S. patent to Schjeldahl which disclosed injection molding a tubular preform and then injecting air into the preform to expand it against a mold (blow molding). The reference did not directly state that the end product balloon was biaxially oriented. It did disclose that the balloon was "formed from a thin flexible inelastic, high tensile strength, biaxially oriented synthetic plastic material." *Id.* at 1462 (emphasis in original). The examiner argued that Schjeldahl's balloon was inherently biaxially oriented. The Board reversed on the basis that the examiner did not provide objective evidence or cogent technical reasoning to support the conclusion of inherency.). *{Emphasis Added}*

. . .

ONCE A REFERENCE TEACHING PRODUCT APPEARING TO BE SUBSTANTIALLY IDENTICAL IS MADE THE BASIS OF A REJECTION, AND THE EXAMINER PRESENTS EVIDENCE OR REASONING TENDING TO SHOW INHERENCY, THE BURDEN

SHIFTS TO THE APPLICANT TO SHOW AN UNOBVIOUS DIFFERENCE

"[T]he PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his [or her] claimed product. Whether the rejection is based on 'inherency' under 35 U.S.C. 102, on 'prima facie obviousness' under 35 U.S.C. 103, jointly or alternatively, the burden of proof is the same...[footnote omitted]." The burden of proof is similar to that required with respect to product-by-process claims. *In re Fitzgerald*, 619 F.2d 67, 70, 205 USPQ 594, 596 (CCPA 1980) (quoting *In re Best*, 562 F.2d 1252, 1255, 195 USPQ 430, 433-34 (CCPA 1977)).

In *In re Fitzgerald*, the claims were directed to a self-locking screw-threaded fastener comprising a metallic threaded fastener having patches of crystallizable thermoplastic bonded thereto. The claim further specified that the thermoplastic had a reduced degree of crystallization shrinkage. The specification disclosed that the locking fastener was made by heating the metal fastener to melt a thermoplastic blank which is pressed against the metal. After the thermoplastic adheres to the metal fastener, the end product is cooled by quenching in water. The examiner made a rejection based on a U.S. patent to Barnes. Barnes taught a self-locking fastener in which the patch of thermoplastic was made by depositing thermoplastic powder on a metallic fastener which was then heated. The end product was cooled in ambient air, by cooling air or by contacting the fastener with a water trough. The court first noted that the two fasteners were identical or only slightly different from each other. "Both fasteners possess the same utility, employ the same crystallizable polymer (nylon 11), and have an adherent plastic patch formed by melting and then cooling the polymer." Id. at 596 n.1, 619 F.2d at 70 n.l. The court then noted that the Board had found that Barnes' cooling rate could reasonably be expected to result in a polymer possessing the claimed crystallization shrinkage rate. Applicants had not rebutted this finding with evidence that the shrinkage rate was indeed different. They had only argued that the crystallization shrinkage rate was dependent on the cool down rate and that the cool down rate of Barnes was much slower than theirs. Because a difference in the cool down rate does not necessarily result in a difference in shrinkage, objective evidence was required to rebut the 35 U.S.C. 102/103 *prima facie* case.

. . .

{Emphasis Added}

As stated in MPEP §2144.03 and supported by case law, the Examiner may also rely upon common knowledge in the art or well known prior art in making a rejection by taking official notice of facts outside the record which are capable of instant and unquestionable demonstration as being "well-known" in the art. The Applicant may seasonably challenge the Examiner's explicit or implicit taking of official notice and require the Examiner to cite a reference or reasoning in support of his or her position. A challenge to the taking of judicial notice must contain adequate information or argument to create on its face a reasonable doubt regarding the circumstances justifying the judicial

notice. When a rejection is based on facts within the personal knowledge of the Examiner, the data should be stated as specifically as possible, and the facts must be supported, when called for by the Applicant, by an affidavit from the Examiner. Such an affidavit is subject to contradiction or explanation by the affidavits of the Applicant and other persons. MPEP §2144.03, states in part:

> **MPEP §2144.03 Reliance on Common Knowledge in the Art or "Well Known" Prior Art**
>
> ***The rationale supporting an obviousness rejection may be based on common knowledge in the art or "well-known" prior art. The examiner may take official notice of facts outside of the record which are capable of instant and unquestionable demonstration as being "well-known" in the art.*** *In re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970) (Board properly took judicial notice that "it is common practice to postheat a weld after the welding operation is completed" and that "it is old to adjust the intensity of a flame in accordance with the heat requirements."). See also *In re Seifreid*, 407 F.2d 897, 160 USPQ 804 (CCPA 1969) (Examiner's statement that polyethylene terephthalate films are commonly known to be shrinkable is a statement of common knowledge in the art, supported by the references of record.).
>
> ***If justified, the examiner should not be obliged to spend time to produce documentary proof. If the knowledge is of such notorious character that official notice can be taken, it is sufficient so to state.*** *In re Malcolm*, 129 F.2d 529, 54 USPQ 235 (CCPA 1942). ***If the applicant traverses such an assertion the examiner should cite a reference in support of his or her position.***
>
> ***When a rejection is based on facts within the personal knowledge of the examiner, the data should be stated as specifically as possible, and the facts must be supported, when called for by the applicant, by an affidavit from the examiner. Such an affidavit is subject to contradiction or explanation by the affidavits of the applicant and other persons.*** See 37 CFR 1.104(d)(2).
>
> ***Applicant must seasonably challenge well known statements and statements based on personal knowledge*** when they are made by the Board of Patent Appeals and Interferences. *In re Selmi*, 156 F.2d 96, 70 USPQ 197 (CCPA 1946); *In re Fischer*, 125 F.2d 725, 52 USPQ 473 (CCPA 1942). See also *In re Boon*, 439 F.2d 724, 169 USPQ 231 (CCPA 1971) (a challenge to the taking of judicial notice must contain adequate information or argument to create on its face a reasonable doubt regarding the circumstances justifying the judicial notice).
>
> . . .
>
> If applicant does not seasonably traverse the well known statement during examination, then the object of the well known statement is taken to be admitted prior art. *In re Chevenard*, 139 F.2d 71, 60 USPQ 239 (CCPA 1943). ***A seasonable challenge constitutes a demand for evidence made as soon as practicable during prosecution. Thus, applicant is charged with rebutting the well known statement in the next reply after the Office action in which the well known statement was made. This is necessary because the examiner must be given the opportunity to provide evidence in the next Office action or explain***

> ***why no evidence is required.*** If the examiner adds a reference to the rejection in the next action after applicant's rebuttal, the newly cited reference, if it is added merely as evidence of the prior well known statement, does not result in a new issue and thus the action can potentially be made final. If no amendments are made to the claims, the examiner must not rely on any other teachings in the reference if the rejection is made final. *{Emphasis Added}*

ii. Scope and Content of Prior Art

A single prior art reference was cited by the Examiner against the claims in issue. The reference is Bacon et al., U.S. Pat. No. 5,440,632, issued on August 8, 1995 ("Bacon et al."). Bacon et al. relates to a method and apparatus for reprogrammable television subscriber service controller for cable or satellite use. The subscriber service controller containing a control microprocessor 128, a memory bus 141, and an asynchronous Flash EPROM 134 coupled to the memory bus 141.

Bacon et al. also details a synchronous detector for the RF signal that is coupled to the RF detection path, an address latch coupled to the microprocessor 128 that stores the address for an memory access to the Flash EPROM 134 and allows the microprocessor 128 to time-wise multiplex its Port C for both address and data transfers, a clock signal, ACLK, that synchronizes data transfer between the multifunction control circuit (MCC) 104 and the microprocessor 128 on a separate serial bus (which is not coupled to the Flash EPROM 134), and a secure microprocessor bus (SMB) 143 containing a clock signal SCLK that is separate from the memory bus 141. *See, e.g.,* Bacon et al. Figures 2A, 2B, 5, and 7, column 6, line 15 to column 7, line 28, column 11, lines 45-66, column 12, lines 16-22, lines 34-37, and column 12, line 62 to column 13, line 4.

Bacon et al. does not teach or disclose a system with a synchronous memory bus coupled to a synchronous non-volatile memory device and, in particular, Bacon et al. does not teach or disclose a synchronous Flash or EPROM memory device with a synchronous interface coupled to a synchronous memory bus as disclosed in the present application.

iii. Analysis

Introduction

In the present application, the Examiner is mistakenly under the impression that memory device behavior arises from the system the memory is placed within and not from the architecture the memory device and/or its interface has been designed to meet. The Examiner is insisting that if a memory device accepts a clock, has synchronous elements, or is engaged by the system it is placed within in a time-wise manner that the memory is a synchronous memory and/or contains a synchronous interface. This broad reading of synchronous/asynchronous memory devices and the Appellant's claims would not be so interpreted by one skilled in the art. The Appellant's specification has defined what synchronous memory devices are and this definition is consistent with the definition of synchronous memory devices in the art. The Examiner's definition is inconsistent with the normal and customary definition of synchronous memory devices. The Appellant has also submitted extrinsic evidence in the form of a separate reference to rebut the Examiner's claim and illustrate the interpretation of one skilled in the art. Further, the Appellant has rebutted each of the Examiner's separate arguments regarding whether the cited reference, Bacon et al., discloses a synchronous memory.

The Appellant has argued during examination that the Examiner has taken official notice or inherently asserted that Bacon et al. disclosed a synchronous memory device. The Examiner has stated that this is not the case and that Bacon et al. expressly discloses a synchronous memory device. As the Appellant asserts herein, the Examiner's rejection of the Appellant's claims under 35 U.S.C. §102(b) as anticipated by Bacon et al. would be in error in either case.

Express disclosure of all elements and claim interpretation

If, as finally asserted by the Examiner in the Advisory Action mailed on May 19, 2004, the Examiner is relying on the express disclosure of Bacon et al. (U.S. Patent 5,440,632) in rejecting the claims 1,2 and 34 under 35 U.S.C. §102(b), the Examiner's rejection is erroneous, as detailed herein.

As stated in MPEP §2131 and supporting case law, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *See, e.g.,* MPEP §2131. In interpreting the

claims at issue in examination, the Examiner must give the broadest reasonable interpretation consistent with the specification. In this the Examiner applies to verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account definitions afforded by the written description contained in applicant's specification. The claims are broadly interpreted during examination utilizing the "plain meaning" of the words, defined as the meaning given to the terms by those of ordinary skill in the art, unless applicant has provided a clear definition in the specification. *See, e.g.,* MPEP §2111 and §2111.01.

In rejecting claims 1, 2 and 34, the Examiner has broadly interpreted the recited synchronous nonvolatile memory device of the claims and memory devices in general as being asynchronous or synchronous dependent on the system they are utilized in regardless of the architecture or interface of the memory device itself. The Appellant asserts that this is contrary to specification and contrary to the plain meaning of the term. As stated above, claims are broadly interpreted during examination utilizing the "plain meaning" of the words. The plain meaning of the words is defined as the meaning given to the terms by those of ordinary skill in the art.

The Appellant asserts that the Examiner has interpreted synchronous memory device or synchronous interface in a manner inconsistent with how it would be interpreted be one skilled in the art. The Appellant has asserted in each response to the Examiner that asynchronous memory devices and synchronous memory devices differ and their interfaces differ, that this is well known in the art, and would be so recognized by those skilled in the art. The Appellant currently asserts, in response to the rationale only finally disclosed by the Examiner in the Advisory Action mailed on May19, 2004, that one skilled in the art would also not interpret a memory device as being asynchronous or synchronous dependent only on the system it is utilized. In support of this, Appellant, as in Appellant's Response to Final of April 30, 2004, recites the extrinsic evidence of Barth et al. (U.S. Patent 6,532,522, Titled: "Asynchronous request/synchronous data dynamic random access memory", Issued: March 11, 2003) to rebut the Examiner's assertion that "the behavior of memory is determined by the system in which the memory is utilized" and support the Appellant's claim that a person of ordinary skill in the art would interpret a synchronous memory device as meaning a

memory device with a synchronous type interface, and how synchronous memory devices differ from asynchronous memory devices:

> In conventional memory systems, the communication between a memory controller and DRAMs is performed through asynchronous communications. For example, the memory controller uses control signals to indicate to the DRAM when requests for data transactions are sent. The data transfers themselves are also performed asynchronously. To meet increased speed requirements, various enhanced asynchronous memory systems have been developed. One such system is the Extended Data Out (EDO) DRAM memory system.
>
> FIG. 1 is a block diagram illustrating a typical EDO DRAM system 100. In the EDO DRAM system 100, data transfers are performed asynchronously in response to control signals and addresses sent from pin buffers 116 of a memory controller to pin buffers 118 of the EDO DRAM over a plurality of lines 120, 122, 124, 134, and 136. Specifically, lines 122 carry an address that is stored in latches 112 and 114. Line 120 carries a row address strobe (RAS) that controls when the address stored in latch 112 is sent to row decoder 106. Line 136 carries a write enable signal that controls timing chains 108 and the direction of data flow on the bi-directional data bus 126.
>
> ...
>
> DRAMs built with an asynchronous RAS/CAS interface have difficulty meeting the high memory bandwidth demands of many current computer systems. As a result, synchronous interface standards have been proposed. These alternative interface standards include Synchronous DRAMs (SDRAMs). In contrast to the asynchronous interface of EDO DRAMS, SDRAM systems use a clock to synchronize the communication between the memory controller and the SDRAMs. Timing communication with a clock allows data to be placed on the DRAM output with more precise timing. In addition, the clock signal can be used for internal pipelining. These characteristics of synchronous communication results in higher possible transfer rates.
>
> FIG. 3 is a block diagram illustrating a conventional SDRAM system 300. In system 300, the memory controller includes a plurality of clocked buffers 304 and the SDRAM includes a plurality of clocked buffers 306. Data from control line 310 and an address bus 312 are received by a finite state machine 308 in the SDRAM. The output of the finite state machine 308 and the address data are sent to memory array 302 to initiate a data transfer operation.
>
> FIG. 4 is a timing diagram that illustrates the signals generated in system 300 during a read operation. At time T0 the memory controller places a read request on line 310 and an address on bus 312. At time T1 the SDRAM reads the information on lines 310 and 312. Between T1 and T2 the SDRAM retrieves the data located at the specified address from memory array 302. At time T2 the SDRAM places data from the specified address on data bus 314. At time T3 the memory controller reads the data off the data bus 314.
>
> Because system 300 is synchronous, various issues arise that do not arise in asynchronous systems. Specifically, the synchronous system has numerous pipeline stages. Unbalanced pipeline stages waste computational time. For example, if a shorter pipeline stage is fed by a longer pipeline stage, there will be some period of time in which the shorter pipeline stage remains idle after

> finishing its operation and before receiving the next set of data from the preceding pipeline stage. Similarly, if a short pipeline stage feeds a longer pipeline stage, the shorter pipeline stage must wait until the longer pipeline stage has completed before feeding the longer pipeline stage with new input.

See, e.g., Barth et al., column 1, lines 21-46, column 2, line 48 to column 3, line 3, and Figures 1, 2, 3 and 4. Appellant further submits that the difference between asynchronous memory types (ROM, DRAM, EEPROM, Flash, and SRAM, etc.) with an asynchronous memory interface and synchronous memory types (SDRAM, DDR, etc.) with a synchronous memory interface are well known in the art. As such, Appellant submits that Barth et al. rebuts the Examiner's assertion that "the behavior of memory is determined by the system in which the memory is utilized" and the assertion that Bacon et al. is a system with a synchronous non-volatile Flash memory and submits that one of ordinary skill in the art would recognize Bacon et al. as describing a non-synchronous memory system.

In light of this, the Appellant respectfully submits that the Examiner has not interpreted the words of the claims at issue in terms of their "plain meaning" or as they would be interpreted by one skilled in the art. The Appellant also submits that, therefore, the Examiner's assertion that "the behavior of memory is determined by the system in which the memory is utilized" is clearly erroneous.

Furthermore, the Appellant asserts that the Examiner has interpreted synchronous memory devices and synchronous memory interfaces in a manner inconsistent with the clear definition thereof in Appellant's specification. These definitions of synchronous memory devices, synchronous interfaces, and systems are disclosed in the Specification at least at Page 2, Lines 11-17, Page 9, Line 23 to Page 10, Line 6, Page 10, Lines 10-19, Page 6, Line 9 to Page 28, Line 20, Page 45, Line 17 to Page 46, Line 28, and Page 47, Lines 3-14.

In particular, the Specification at Page 45, Line 17 to Page 46, Line 28 states, in part:

> As explained above, many processor/computer systems use a code that is stored on a hard disk, copied to the DRAM and executed from the DRAM. This is done because the speed and performance of the system is usually dictated by the performance of the DRAM. Most of today's systems use SDRAM because it is synchronous and runs at speeds exceeding 100MHz.

> The main reason for using DRAM rather than using prior Flash memories is based on cost and performance. The cost to the system is two fold. First, both Flash memories as well as DRAM would have to be purchased. Secondly, the system cannot put the Flash memory on the main memory bus since prior Flash memories do not work in the same manner as a DRAM, and DRAM controllers are not designed to handle the extra control inputs required for today's Flash memory devices. Transferring data from a hard disc to SDRAM takes time. This boot time is often very irritating to computer users.
>
> The Flash memory described herein, however, uses the same interface as a DRAM for reading. This flash memory uses the same interconnect pins as a SDRAM and fits into the same package. . . .
>
> The Flash read obviously needs to have the same performance as a SDRAM chip. Current flash memories are running as fast as 10 to 50MHz, which is much slower than the performance one gets out of SDRAM chips. The present invention provides the same performance as the SDRAM, and allows system designers to put this flash memory on the main memory bus. Thus, reducing the pin cost on their controller as well as avoiding the need to support another bus. . . . Regarding performance, the present flash memory eliminates the time needed to upload the SDRAM at power up and allows for an instant turn on of the system.
>
> In summary, the present invention provides a flash memory device that has the same interconnect pin configuration as a synchronous DRAM and fits into the same package. . . .
>
> Figure 32 illustrates a block diagram of a system 300 according to one embodiment of the invention. The system includes a synchronous flash memory 320 coupled to a memory controller 340 via a main memory bus 330. The main memory bus can also be coupled to a DRAM 350.

The Appellant has thus defined synchronous memory devices, synchronous nonvolatile memory devices, synchronous memory interfaces, and systems with synchronous memory buses in a manner consistent with their ordinary and customary meanings. The Examiner therefore may not provide an alternative and inconsistent interpretation. The Appellant also notes that the Specification from Page 45, Line 17 to Page 46, Line 28 has also defined, in describing that prior Flash memory devices cannot be placed on the memory bus as synchronous DRAM, that memory devices will not work synchronously or asynchronously depending on the system they are utilized in, contrary to the Examiner's assertion. Thus, the Appellant respectfully submits that the Examiner has not interpreted the words of the claims at issue in terms of how they were express;y defined in the Appellant's Specification and that therefore the Examiner's rejection of claims 1, 2 and 34 under 35 U.S.C. §102(b) over Bacon et al. is clearly erroneous.

In addition, the Appellant maintains that each of the Examiner's examples of synchronous behavior of the system described in Bacon et al. do not disclose a system

operating in a synchronous manner in association with a synchronous nonvolatile memory. The Examiner stated in the Advisory Action of May 19, 2004, that "[t]he rejection describes no less than four clear examples of synchronous behavior in the Bacon et al. system in which the memory 134 is utilized. None of the applicant's arguments directed towards these examples are deem convincing, since each of these arguments appear to rely on the applicant's recurring 'inherency' argument." The Appellant disagrees with this assertion and maintains that the Appellant responded to each of the Examiner's four examples independent from the argument of inherent synchronous operation. As stated in Appellant's Response to Final of April 30, 2004:

> In addition, the Applicant specifically responds to the portions of Bacon et al. raised by the Examiner as supportive of Bacon et al. disclosing a synchronous system. Regarding (a), the use of a synchronous detector 105 in column 7, line 7 of Bacon et al., the Applicant notes that the synchronous detector 105 is coupled to the RF detection path and input of the subscriber terminal of a subscription television system in FIG. 2 and is not directly coupled to the EROM/Flash 134 or microprocessor 128. The "audio signal is converted from the 41.25 Mhz IF carrier to the intermodulation frequency of 4.5 Hz by synchronous detector 105." *See, e.g.,* Bacon et al. Figures 2A and 2B, column 6, line 15 to column 7, line 28, and column 7, lines 5-7.
>
> Regarding (b), the Examiner noted, "column 11, lines 45 et seq., which state 'The microprocessor 128 time multiplexes the port C lines to be both address and data lines AD0-A7 and applies the to a data latch 202 which maintains the address word while to reads data from the same lines. The address lines are applied to the address inputs A0-A15 of the internal memory 134, in FIG. 5 a 256k Flash EPROM (pages 0-3).' Time multiplexing is a synchronous activity." The Applicant maintains that, Bacon et al. column 11, lines 45 et seq. discloses a microprocessor coupled to an external latch 202, as shown in FIG. 5, that holds the lower portion of the address (A0-A7) to be accessed in the memory 134 so that the port C of the microprocessor 128 can be reused to transmit or receive data to/from the memory 134. While this activity may be constrained to occur in a sequential fashion (load address in latch 202 to access a location in memory 134, read/write memory 134), the Applicant maintains that this does not state that the

memory is synchronous or even that the interaction with the data latch and following access to the memory 134 occur in a synchronous manner; all that is required is that the data latch 202 be loaded with the lower portion of an address (A0-A7) before the memory 134 is accessed. In addition, the Applicant maintains that the statement "[t]he microprocessor 128 timewise multiplexes port C lines to be both address and data lines AD0-AD7 and applies them to data latch 202 which maintains the address word while it reads data from the same lines," only refers to the timewise dual use of the lines of microprocessor port C, and not that the interaction of the microprocessor 128 and memory 134 being synchronous. *See, e.g.*, Figure 5 and column 11, lines 45-59.

Regarding (c), the Examiner noted, "column 11, lines 63 et seq., which state 'An address clock on line ACLK provides a clock signal to synchronize the transfer of data between the microprocessor 128 and MCC 104." The Applicant maintains that, while this may indicate that data transfer between the microprocessor 128 and the multifunction control circuit (MCC) 104 of the subscriber system, this does not state or suggest that the memory 134 is a synchronous non-volatile memory or has a synchronous memory interface.

Regarding (d), the Examiner noted, "column 12, lines 18 et seq., which state 'The SMB comprises 4 input/output data lines SD0-SD3 and a serial clock line SCLK to time the communications. The memory controller 112 additionally provides a master clock.'" The Applicant notes that the secure microprocessor bus (SMB) 143 is not coupled to Flash EPROM 134 in FIG. 5 of Bacon et al., and is only shown coupled to the MCC 104, the secure microprocessor 136, and the memory extension connector 200. The Applicant maintains that this does not disclose that the memory 134 is a synchronous non-volatile memory or has a synchronous memory interface. Furthermore, the Applicant notes that Bacon et al. discloses SCLK is for serial clocking and that the expansion connector 200 allows another secure microprocessor 201 to be coupled to the SMB bus 143 to supplement or override the secure microprocessor 136. *See, e.g.*, Figures 5 and 7, column 12, lines 16-22, lines 34-37, and column 12, line 62 to column 13, line 4.

Inherent disclosure of elements in cited reference

If, as initially responded to by the Appellant, the Examiner is relying on the inherent disclosure of Bacon et al. in rejecting the claims 1,2 and 34 under 35 U.S.C. §102(b), or is taking official notice of Bacon et al. disclosing a synchronous system the Examiner's rejection is also erroneous, as detailed below.

Inherent elements of a prior art reference may also be used in rejecting claims under 35 U.S.C. §102 or §103. To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art. Once the examiner makes a prima facie case for an element being inherent, the burden shifts to the applicant to refute the case for inherency by reasoning or by providing extrinsic evidence. *See, e.g.,* MPEP §2112.

As stated in Appellant's Response to Final of April 30, 2004, the Appellant notes that nowhere does Bacon et al. specifically disclose that its Flash or EPROM is capable of synchronous operation or has a synchronous interface. If, contrary to the Examiner's assertion, the Examiner maintains that "the behavior of memory is determined by the system in which the memory is utilized" is an inherent feature of Bacon et al., the Appellant respectfully submits that the Examiner has the burden of proving that the inherent element must of necessity only work in the manner of the Appellant's disclosed invention. If any other interpretation is possible for the inherent element relied upon for the rejection, the rejection cannot be maintained. (*See,* MPEP §2112 and §2163.07(a)). "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). (*See,* MPEP §2112).

Appellant respectfully submits that the allegedly inherent characteristic of a synchronous non-volatile memory system or a memory that operates in a synchronous or

asynchronous manner dependent on the memory system it is utilized in does not necessarily flow from the teachings of the applied prior art of Bacon et al. and would be so recognized by persons of ordinary skill. In other words, there is no support that a system containing a synchronous component or a system with a memory that accepts a clock signal necessarily implies that the memory of the system is inherently a memory of a synchronous type and has a synchronous type of interface. Appellant also submits that there are multiple possible interpretations for the fact that the memory system has a synchronous component or has a memory that accepts a clock signal, besides the conclusion that the memory of the system is inherently a memory of a synchronous type and/or has a synchronous type of interface.

A system is not synchronous because it is tied to a clocked processor. If so, all memory would be considered synchronous.

One possible alternative interpretation is that the memory of Bacon et al. interfaces to an external system that has a synchronous RF audio signal (a television signal that time-wise multiplexes video and audio) and therefore must have a synchronous detector as a component to detect and isolate the audio component of the signal. As such, because of the fact that a person of ordinary skill in the art would not recognize that the system of Bacon et al. would necessarily be a synchronous memory system or contain a synchronous memory device, and that there are multiple possible interpretations to the system of Bacon et al. having a synchronous non-memory component or a memory that accepts a clock, the Examiner has not shown the necessity required for inherency in claiming Bacon et al. describes a synchronous non-volatile memory system or having a synchronous non-volatile memory. Therefore as Bacon et al. does not inherently describe a synchronous non-volatile memory system or having a synchronous non-volatile memory, the Appellant submits that Bacon et al. fails the all element rule for Appellant's independent claims 1 and 34.

Appellant also submits that if the Examiner maintains that Bacon et al. inherently describes a synchronous non-volatile memory system or as inherently having a synchronous non-volatile memory, that such inherency may be rebutted by the Appellant by the submission of extrinsic evidence to the contrary. A *prima facie* case of inherency by the Patent Office may be rebutted by the Appellant by an appropriate showing. "When the PTO shows a sound basis for believing that the products of the Appellant and

the prior art are the same, the Appellant has the burden of showing that they are not." *In re Spada*, 911 F.2d 705, 709, 15 USPQ2d 1655, 1658 (Fed. Cir. 1990). (*See,* MPEP §2112.01). Therefore, the *prima facie* case can be rebutted by evidence showing that the prior art products do not necessarily possess the characteristics of the claimed product. *In re Best*, 562 F.2d at 1255, 195 USPQ at 433. (*See*, MPEP §2112.01).

Appellant respectfully submits that the Application utilizes the term "synchronous" in claims 1-2 and 34 of the present application to refer to a memory type that incorporates a synchronous interface. In other words, a memory of a type where the interface has a defined timing and the data is placed on or read from the memory interface at a specified time during a data access interaction with the memory. Appellant submits that such is explained in the Application as originally filed. *See*, Application, Page 2, Lines 11-17. Appellant respectfully submits that a person of ordinary skill in the art would interpret a synchronous memory device as meaning a memory device with a synchronous interface as described by Appellant above.

In support of this, as above, Appellant recites the extrinsic evidence of Barth et al. (U.S. Patent 6,532,522, Titled: "Asynchronous request/synchronous data dynamic random access memory", Issued: March 11, 2003) to rebut the Examiner's argument of inherency and support the Appellant's claim that a person of ordinary skill in the art would interpret a synchronous memory device as meaning a memory device with a synchronous type interface. *See, e.g.,* Barth et al., column 1, lines 21-46, column 2, line 48 to column 3, line 3, and Figures 1, 2, 3 and 4. As such, Appellant submits that Barth et al. rebuts the Patent Office's assertion that Bacon et al. is inherently a system with a synchronous non-volatile (EPROM/Flash) memory and submits that one of ordinary skill in the art would recognize Bacon et al. as describing a non-synchronous memory.

Official Notice

The Examiner may also rely upon common knowledge in the art or well known prior art in making a rejection by taking official notice of facts outside the record which are capable of instant and unquestionable demonstration as being "well-known" in the art. The Applicant may seasonably challenge the Examiner's explicit or implicit taking of official notice and require the Examiner to cite a reference or reasoning in support of his or her position. A challenge to the taking of judicial notice must contain adequate

information or argument to create on its face a reasonable doubt regarding the circumstances justifying the judicial notice. When a rejection is based on facts within the personal knowledge of the Examiner, the data should be stated as specifically as possible, and the facts must be supported, when called for by the Applicant, by an affidavit from the Examiner. Such an affidavit is subject to contradiction or explanation by the affidavits of the Applicant and other persons. *See, e.g.,* MPEP §2144.03.

If the Examiner is, alternatively, taking official notice of Bacon et al. disclosing Flash or EPROM that is synchronous/has a synchronous interface or that "the behavior of memory is determined by the system in which the memory is utilized," as stated in the Advisory Action of May 19, 2004. The Appellant has effectively seasonably challenged the Examiner's explicit or implicit taking of official notice in the responses of March 3, 2004 and April 30, 2004 and required the Examiner to cite a reference or reasoning in support of his or her position. The Appellant notes that sufficient information or argument was given in the Appellant's responses of March 3, 2004 and April 30, 2004 to create on its face a reasonable doubt regarding the circumstances justifying any official notice by the Examiner regarding this matter. The Appellant also notes that the Examiner failed to provide any reasoning in support of his position until the Advisory Action of May 19, 2004. The Appellant maintains that for the reasons listed above in regards to anticipation with explicit or inherent elements, that any taking of official notice is herein rebutted and that claims 1, 2 and 34 are therefore deemed allowable.

The Claims

Appellant's claim 1 is directed to a computer system comprising a memory controller, a main memory bus coupled to the memory controller, and a synchronous non-volatile memory device coupled to the main memory bus. As Bacon et al. does not describe a system having a synchronous non-volatile memory device, Bacon et al. does not teach or disclose all elements of claim 1.

Appellant's claim 2 depends from claim 1 and is directed to a computer system as described in claim 1, wherein the synchronous non-volatile memory device has a command interface comprising a write enable connection (WE#) to receive a write enable signal, a column address strobe connection (CAS#) to receive a column address strobe signal, a row address strobe connection (RAS#) to receive a row address strobe signal,

and a chip select connection (CS#) to receive a chip select signal. As Bacon et al. does not describe a system having a synchronous non-volatile memory device or a synchronous command interface, Bacon et al. does not teach or disclose all elements of claim 2.

Appellant's claim 34 is directed to a computer system comprising a memory controller, a main memory bus coupled to the memory controller, and a synchronous non-volatile memory device coupled to the main memory bus, the synchronous non-volatile memory having a command interface. The command interface comprising a write enable connection (WE#) to receive a write enable signal, a column address strobe connection (CAS#) to receive a column address strobe signal, a row address strobe connection (RAS#) to receive a row address strobe signal, and a chip select connection (CS#) to receive a chip select signal. As Bacon et al. does not describe a system having a synchronous non-volatile memory device or a synchronous command interface, Bacon et al. does not teach or disclose all elements of claim 34.

As such, since Bacon et al. does not describe a synchronous non-volatile/Flash memory device, each and every limitation of the claims 1, 2 and 34 is not present in Bacon et al., and the rejection is improper. Claims 1, 2 and 34 are allowable.

Appellant respectfully contends that claims 1, 2 and 34 have been shown to be patentably distinct from the cited reference. Accordingly, Appellant requests the Examiner's final rejection under 35 U.S.C. § 102(b) be reversed and requests reconsideration and allowance of claims 1, 2 and 34.

B. Objection of the drawings under 37 C.F.R. §1.84(u)(1)

i. The Applicable Law

As stated in MPEP §608.02(e), the Examiner determines the completeness and consistency of the drawings. The drawings must meet the requirements of 37 C.F.R. §1.84 and, in particular the drawing views must be numbered according to 37 C.F.R. §1.84(u)(1), which states:

1.84(u) *Numbering of views.*

> (1) The different views must be numbered in consecutive Arabic numerals, starting with 1, independent of the numbering of the sheets and,

> if possible, in the order in which they appear on the drawing sheet(s). Partial views intended to form one complete view, on one or several sheets, must be identified by the same number followed by a capital letter. View numbers must be preceded by the abbreviation "FIG." Where only a single view is used in an application to illustrate the claimed invention, it must not be numbered and the abbreviation "FIG." must not appear.
>
> (2) Numbers and letters identifying the views must be simple and clear and must not be used in association with brackets, circles, or inverted commas. The view numbers must be larger than the numbers used for reference characters.

In addition, MPEP §507(E) states that drawings are subject to initial review by the Office of Initial Patent Examination, which states in part:

> Under the OIPE review process, OIPE may object to and require corrected drawings within a set time period, if the drawings:
>
> . . .
>
> (E) have more than one figure and each figure is not labeled "Fig." With a consecutive Arabic numeral (1, 2, etc.) or an Arabic numeral and capital letter in the English alphabet (A, B, etc.). See 37 CFR 1.84(u)(1);
>
> . . .

ii. Analysis

The Examiner in the Advisory Action mailed May 19, 2004 that the substitute drawings were disapproved for failing to comply with 37 C.F.R. §1.84(u)(1). The Examiner stated that the drawing views were required to be labeled "FIG." by 37 C.F.R. §1.84(u)(1) instead of the Appellant's "Fig." labeling.

Appellant notes that 37 C.F.R. §1.84(u)(1) only states that the drawing views be labeled with the term "Fig." And, while it uses an all capitalized form, does not explicitly state or require this. The Appellant further notes that MPEP §507(E) states that the drawing views should only be required to include the Appellant's form of label "Fig." and also does not require the all capitalized form insisted upon by the Examiner. The Appellant therefore maintains that given the lack of an explicit requirement for labeling and in view of the inconsistent requirements of 37 C.F.R. §1.84(u)(1) and MPEP §507(E), the Examiner's insistence on a given labeling style is unreasonable.

The Appellant therefore requests that the Examiner's objection be reversed and the substitute drawings be accepted.

X. Conclusion

Appellant has set forth reasons why the Examiner is incorrect in maintaining his rejections of the pending claims. In regards to claims 1, 2 and 34, rejected in view of Bacon et al. under 35 USC §102(b); as the Examiner has not used the plain meaning of the term "synchronous nonvolatile memory" and as Bacon et al. does not describe a synchronous non-volatile/Flash memory device, each and every limitation of the claims 1, 2 and 34 are not present in Bacon et al., and the rejection is improper. Therefore claims 1, 2 and 34 are allowable.

The Examiner has also failed to set forth a *prima facie* case of inherency of the reference Bacon et al. in regards to teaching a synchronous memory device. Bacon et al. does not support a conclusion that its disclosed memory devices are synchronous or have a synchronous interface or that one of ordinary skill in the art would have concluded it was such. Further, the cited references of Bacon et al. does not teach or suggest all the claim limitations of Appellant's claims 1, 2 and 34.

In addition, the Examiner's reasons for requiring the drawing views to be labeled "FIG." instead of the Appellant's "Fig." label under 37 C.F.R. §1.84(u)(1) are inconsistent and unreasonable.

Appellant respectfully submits that, for the above reasons, claims 1, 2 and 34 are allowable over the cited art. Therefore, reversal of the Examiner's rejections and allowance of the claims is respectfully requested. The Appellant also respectfully requests reversal of the Examiner's objection to the Appellant's labeling of drawing views in the submitted formal drawings.

For at least the reasons discussed above, Appellant submits that the pending claims are patentable. Accordingly, Appellant requests that the Board of Appeals reverse the Examiner's decisions regarding the claims.

Respectfully submitted,

Date: 8/10/04

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APPENDIX A
CLAIMS ON APPEAL

1. (original) A computer system comprising:

a memory controller;

a main memory bus coupled to the memory controller; and

a synchronous non-volatile memory device coupled to the main memory bus.

2. (original) The computer system of claim 1, wherein the synchronous non-volatile memory device has a command interface comprising:

a write enable connection (WE#) to receive a write enable signal;

a column address strobe connection (CAS#) to receive a column address strobe signal;

a row address strobe connection (RAS#) to receive a row address strobe signal; and

a chip select connection (CS#) to receive a chip select signal.

3-26. (cancelled)

27. (withdrawn) The computer system of claim 1, wherein the synchronous non-volatile memory device contains a Vccp power supply connection.

28. (withdrawn) The computer system of claim 1, wherein the synchronous non-volatile memory device further comprises a package having a plurality of interconnect pins corresponding to the external connections.

29. (withdrawn) The computer system of claim 28, wherein the synchronous non-volatile memory device further comprises a plurality of interconnect pins which are physically arranged in a pattern compatible with a synchronous dynamic random access memory (SDRAM).

30. (withdrawn) The computer system of claim 1, wherein the synchronous non-volatile memory device further comprises a package having a plurality of conductive interconnect locations corresponding to external connections of the synchronous non-volatile memory device to the main memory bus.

31. (withdrawn) The computer system of claim 30, wherein the conductive interconnect locations are physically arranged in a pattern compatible with a synchronous dynamic random access memory (SDRAM).

32. (withdrawn) The computer system of claim 31, wherein the synchronous non-volatile memory device operates within read timing specification parameters for an SDRAM.

33. (withdrawn) The computer system of claim 1, wherein the synchronous non-volatile memory device is one of a synchronous flash memory device and a synchronous EEPROM memory device.

34. (original) A computer system comprising:

a memory controller;

a main memory bus coupled to the memory controller; and

a synchronous non-volatile memory device coupled to the main memory bus, the synchronous non-volatile memory having a command interface, where the command interface comprises:

a write enable connection (WE#) to receive a write enable signal;

a column address strobe connection (CAS#) to receive a column address strobe signal;

a row address strobe connection (RAS#) to receive a row address strobe signal; and

a chip select connection (CS#) to receive a chip select signal.

35. (withdrawn) The computer system of claim 34, wherein the synchronous non-volatile memory device has conductive interconnect locations which are

physically arranged in a pattern compatible with a synchronous dynamic random access memory (SDRAM).

36. (withdrawn) The computer system of claim 34, wherein the synchronous non-volatile memory device operates within read timing specification parameters for an SDRAM.

37. (withdrawn) The computer system of claim 34, wherein the synchronous non-volatile memory device is a one of a synchronous flash memory device and a synchronous EEPROM memory device.

38. (withdrawn) The computer system of claim 34, wherein the synchronous non-volatile memory device comprises a plurality of external connections comprising:

a plurality of bi-directional data connections;

a plurality of memory address connections;

a clock input connection;

a clock enable connection;

a plurality of memory array bank address connections;

power supply connections;

a plurality of data mask connections;

a reset connection; and

a Vccp power supply connection.